SPECIFICATIONS AND FEATURES

DATASHEET

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UFirebird-UC6226NIS (E310E2)

GNSS Positioning Chip

Revision History

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R1.0	First release	Feb. 2023

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Foreword

This datasheet offers you information in the features of the hardware, installation, specification and use of UNICORECOMM UC6226NIS-E310E2 chip (hereinafter referred to as UC6226NIS-E2).

Readers it applies to

This datasheet is applied to technicians who know GNSS receivers to some extent but not to the general readers.

Contents

Chapter 1

1. Functional Characteristics

1.1. Overview

Figure 1-1 UFirebird UC6226NIS-E2 Chip

UNICORECOMM UFirebird™ (UC6226NIS-E2) is designed with 28nm process and efficient PMU, features low power consumption and ultimate compact size, which significantly increase the battery life of user equipment.

UC6226NIS-E2 is suitable for global applications, supports GPS, GLONASS, BDS, Galileo and multi-system positioning, as well as supports a variety of SBAS signal reception processing, thus providing users with fast and accurate high-performance positioning experience.

UC6226NIS-E2 can connect with the gyroscope, accelerometer, and other sensors to realize fusion positioning. With the accurate scenes and pattern recognition, in the harsh signal environment, UC6226NIS-E2 can still ensure fast and accurate positioning effect, and significantly reduce the average operating power consumption, substantially increase the standby time of devices, such as mobile phones, wearing devices and Internet of Things devices.

What's more, UC6226NIS-E2 has adopted the high integration design, and the chip has provided built-in DC/DC, LDO, LNA and RTC, etc. With the simple peripheral devices, it can achieve a complete GNSS receiver function, which can significantly reduce the PCB area and save hardware costs for users.

UC6226NIS-E2 QFN40 package is compatible with mainstream package.

1.2. Features

UC6226NIS-E2 has the following features:

- Positioning engine features
  - 64-channel simultaneous tracking;
  - Less than 1 second hot start time;
  - -147 dBm cold start sensitivity, -160 dBm tracking sensitivity;
  - Up to 5Hz data update rate
- Supports GPS, BDS, GLONASS and Galileo
- Supports 26MHz TCXO;
- Supports external 32.768kHz crystal;
- Built-in DC/DC and power management unit;
- Supports ROM built-in firmware and Flash expansion firmware
- Industrial grade[1] 5.0mm x 5.0mm QFN40 package, 0.4mm pitch

1.3. Performance Specifications

GNSS performance of the UC6226NIS-E2 chip is as follows:

Table 1-1 UC6226NIS-E2 GNSS Performance

Item	Description
Positioning accuracy	
Single point positioning	<2.0m[2]
Velocity accuracy	0.1m/s
Sensitivity[3]	
	GNSS
Cold Start[4]	-147dBm
Tracking	-160dBm

[1] Only supports -30°C~+85°C.

[2] CEP, 50%

[3] The sensitivity index needs C/N0 attain 41dB when the signal strength is -130dBm

[4] Externally matches LNA to ensure superior performance

Hot start	-154dBm
Reacquisition	-158dBm
TTFF[5]	
Cold start	<28s
AGNSS	<4s[6]
Hot start	<1s
Reacquisition	<1s

1.4. System Block Diagram

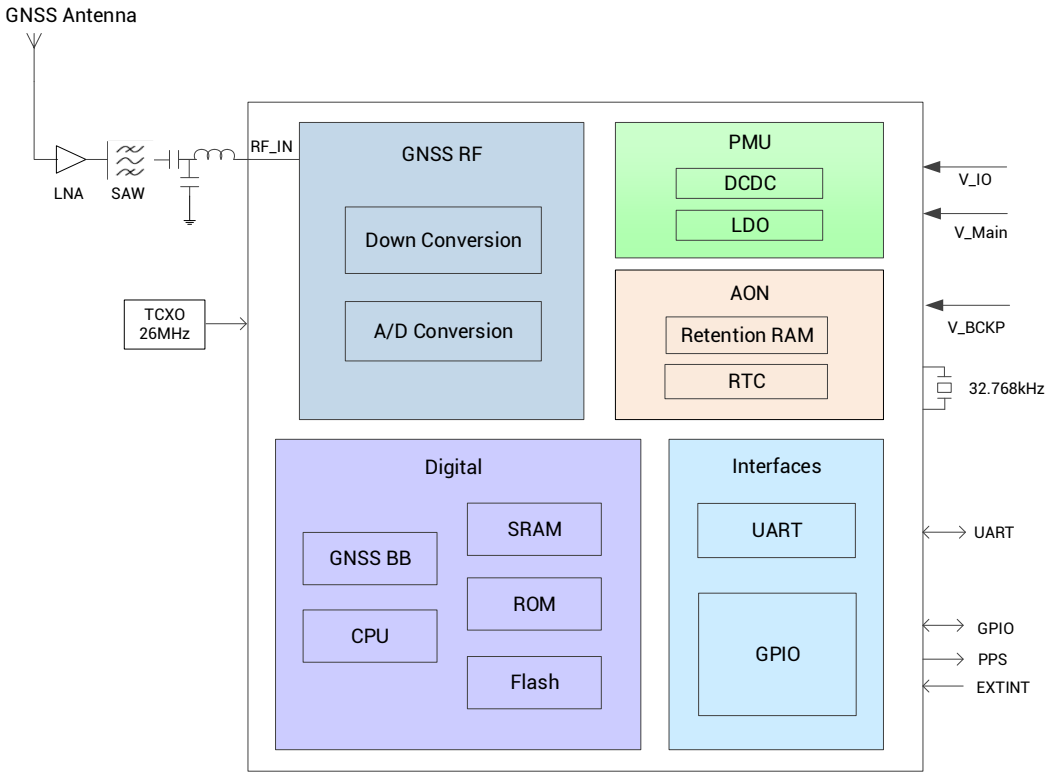


Figure 1-2 UC6226NIS-E2 chip block diagram

1.5. Satellite Navigation Systems

UC6226NIS-E2 supports multiple GNSS systems, including GPS, BDS, GLONASS and Galileo. RF uses a broadband design that simultaneously receives and processes satellite signals

[5] Satellite signal strength is up to -130dBm

[6] Prompt injection of assisted ephemeris

from multiple satellite systems, including GPS L1, BDS B1, GLONASS L1 and Galileo E1, which can receive or process two or three of them in parallel.

1.5.1. GPS

UC6226NIS-E2 can receive and track GPS L1 signal at 1575.42 MHz.

1.5.2. GLONASS

UC6226NIS-E2 can receive and track GLONASS L1 signal, the signal frequency is 1602 MHz + k * 562.5 kHz, k = -7 ~ +6. Users can design GLONASS receivers in compliance with regulatory requirements.

1.5.3. BDS

UC6226NIS-E2 can receive and track the BDS satellite navigation system's 1561.098 MHz B1 signal. It can combine with GPS to receive and track the BDS B1 satellite signal, increase the coverage, improve reliability and improve accuracy.

1.5.4. Galileo

UC6226NIS-E2 can simultaneously receive and track GPS and Galileo signals, as well as enhance accuracy and coverage.

1.6. Protocols and Interfaces

UC6226NIS-E2 data protocol complies with “Unicore Protocol” specification. By default, the chip communicates with host device via UART. For the technical parameters of the various protocols, supported communication interfaces and firmware versions, please refer to the *Unicore Protocol* documentation.

1.6.1. Terms and Abbreviations

The following table lists the terms and abbreviations involved or used in this document:

Table 1-2 List of terms and abbreviations

Abbreviations	Complete Description or Name
A/D	Analog/Digital
ADC	Analog Digital Convertor
AGC	Automatic Gain Control

Abbreviations	Complete Description or Name
AGNSS	Assisted GNSS
BB	Baseband
CP	Chip Probing
DC/DC	Direct Current to Direct Current
DGNSS	Differential GNSS
FT	Final Test
Galileo	Galileo Navigation Satellite System
GLONASS	Global Navigation Satellite System
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
LDO	Low DropOut regulator
LNA	Low Noise Amplifier
PDR	Pedestrian Dead Reckoning
PGA	Programmable Gain Amplifier
PIO	Programming Input/Output
PLL	Phase Locked Loop
PMU	Power Management Unit
POR	Power On Reset
RAM	Random Access Memory
RF	Radio Frequency
RTC	Real-Time Clock
SBAS	Satellite-Based Augmentation System
SAW	Surface Acoustic Wave
SPI	Serial Peripheral Interface
SQI	Serial Quad I/O
TCXO	Temperature Compensate Crystal Oscillator

Chapter 2

2. RF Subsystem

RF subsystem adopts wideband design. The input signal is centered at about 1575MHz with a 100 MHz band width. The received GNSS signals are amplified by a Low Noise Amplifier (LNA), and then fed to a gain block, which offers further amplification, thus reducing the noise figure requirements for the mixer. The gain block also provides a single-ended to differential conversion.

After the complex down-conversion, the multi-GNSS signals are split up into I and Q channels. Afterwards both channels are I/Q low-pass filtered and amplified by separate Programmable Gain Amplifiers (PGA). The amplified I and Q signals will do the A/D conversion to get 6-bits I/Q digital signals that are then sent to baseband section, where signal processing and final image rejection take place.

2.1. LNA

The low noise amplifier (LNA) makes use of a single stage configuration and requires external matching to function satisfactorily. For improved performance, an external LNA should be added, of which the gain range is recommended to be within 17dB~45dB. Moreover, it is necessary to use an external SAW filter to suppress out-of-band interference.

2.2. Gain Block

A single stage differential amplifier follows the LNA providing further amplification and conversion from single-ended to differential signaling.

2.3. Mixer

UC6226NIS-E2 uses the active I/Q mixer to first convert the multi-GNSS signals to an intermediate frequency. At this stage the signals are split into two similar IF channels. Both channels are further amplified and converted into different GNSS signal band.

2.4. I/Q Low-Pass Filter (LPF)

The low-pass filter removes any high-frequency from the desired signal. For single GNSS system signal reception, their cut-off frequency and band width are adjusted lower to reduce power consumption.

2.5. PGA

The programmable gain amplifiers (PGA) are used to provide the ADCs with appropriate input IF signals. The PGA gain is automatically looped and adjusted based on the ADC output signal values, providing an automatic gain control (AGC) for the receiver.

PGA gain can be configured as a fixed value via GPIO to improve system's robustness, which is suitable for applications that integrate with mobile communication functions.

2.6. ADC

Two 6-bit ADCs are used for A/D conversion in the chip. I and Q-branch ADCs output 6-bit signals respectively, which then enter into baseband subsystem for processing.

Chapter 3

3. Baseband Subsystem

3.1. Interfaces

The digital I/O of the baseband section is powered by VDD_IO, and the VDD_IO level is the same as applied logic voltage level. Without supplying VDD_IO, the chip will not work.

As the chip's selected digital IO does not support anti-current backflush function, IO interface should not be supplied power separately in the case of power down in the actual application. Please see the note in 3.2 for details.

3.1.1. UART

UC6226NIS-E2 makes use of two UART interfaces, UART1 and UART2, which can be used for communication with a host. Both of them support configurable baud rates up to 921600bps.

By default, PIO6/PIO7 corresponds with UART1, which is the main UART port in standard firmware version. The communication interface of the chip can be mapped to a different PIO interface via D_SEL. PIO6/PIO7 can also be used as an SPI, at which point UART1 will be mapped to PIO15/PIO16. Refer to the note in 3.2 for D_SEL usage and corresponding communication interface mapping.

UART2 can use PIO17/PIO18, or PIO10/PIO12, or PIO2/PIO3. By default, UART2 will use PIO17/PIO18 in the standard firmware. UART2 is mainly used for transmitting or debugging auxiliary information.

3.1.2. SPI

SPI is reserved and is not supported currently.

3.2. PIO

The PIO module may be configured as a GPIO or as the aforementioned communication interface. The following table describes all PIO functions.

Table 3-1 PIO functions

PIO #	Default Function	I/O	Description	Alternate Function
0	GPIO	I/O	NC	
1	GPIO	I/O	NC	
2	GPIO	I/O	NC	TIMEPULSE, UART2 TX
3	GPIO	I/O	NC	TIMEPULSE, UART2 RX
4	GPIO	I/O	NC	
5	GPIO	I/O	NC	
6	TX1	O	UART1 TX (if D_SEL is high at startup)	GPIO
7	RX1	I	UART1 RX (if D_SEL is high at startup)	GPIO
8	GPIO	I/O	NC	SCL
9	GPIO	I/O	NC	SDA
10	D_SEL	I	Communication interface selection pin. This pin forces a pull up by default	
11	TIMEPULSE	O	1PPS output	EVENT
12	BOOT_MODE	I	Bootstrap mode selection pin. This pin forces a pull up by default	UART1 TX, UART2 TX
13	GPIO	I	No function by default	EVENT, UART1 CTS, SCL
14	No function	I	Can be configured as antenna detection input	EVENT, ANT_DET
15	ANT_OK	I	Antenna status detection input	ANT_SHORT

PIO #	Default Function	I/O	Description	Alternate Function
16	ANT_OFF	O	Antenna power supply control output and output state is related to the PIO15 state	SPD_PULSE
17	UART2 RX	I	UART2 RX	SCL
18	UART2 TX	O	UART2 TX	UART2 TX SDA

☞ *As the digital IO selected by UC6226NIS-E2 does not support anti-current backflush function, please pay attention to the following points in development and application:*

1) When VDD_IO and V_DCDC_IN/V_CORE use the same power supply: users should pay attention to the signal state of host port that communicates with UART and functional ports connected with UC6226NIS-E2 when power down. If host computer wants to control the chip power down, users should first set the ports that connect with the chip to high impedance state so as to prevent the chip from consuming host computer's power or failing to start up.

2) In case VDD_IO and V_DCDC_IN/V_CORE do not use the same power supply, users can cut off V_DCDC_IN/V_CORE power supply to achieve the purpose of chip power-down.

3.3. Watchdog

UC6226NIS-E2 includes a watchdog timer, which prevents system-lockups caused when the software gets trapped in a deadlock. During normal operation, the firmware resets the watchdog's internal counter at regular intervals before timer overflow occurs.

3.4. Timer Counter

The timer counter has one TIMEMARK input and one TIMEPULSE output. TIMEMARK can be input via PIO11, PIO13 or PIO14, but only be input through one of the PIOs. TIMEMARK inputs (routed through EXTINT0 and EXTINT1) is timestamp events relative to GPS time.

TIMEPULSE can be output via PIO2, PIO3 or PIO11, but only one TIMEPULSE can be output at one time. TIMEPULSE outputs generate pulse sequence synchronized with GPS or UTC time grid, time intervals can be configured over a wide frequency range.

3.5. Clock

3.5.1. TCXO

The chip requires an external 26MHz clock, which can be provided by TCXO, providing reference frequency for RF and baseband PLLs.

3.5.2. PLL

The fully integrated, low-power PLL generates the system clock from the 26MHz reference frequencies supplied by TCXO.

3.5.3. RTC

The RTC is driven internally by a 32.768 kHz oscillator, which makes use of an external 32.768 kHz crystal.

If the main supply voltage and IO power supply fail and a backup battery is connected to V_BCKP, the baseband, RF, CPU will switch off, but the RTC still runs providing a timing reference for the receiver. This operating mode is called RTC puncturing mode. Under the RTC puncturing mode, the relevant data are still saved in the Retention RAM.

The RTC puncturing mode is required for GNSS hot start function. If RTC is abnormal, it will affect the performance of hot start.

If Retention RAM and RTC are not used, UC6226NIS-E2 does not require a backup battery, and V_BCKP has to be connected to VDD_IO.

The standard firmware supports 32.768 kHz by default. And the chip also supports external digital clock signal of 32.768 kHz directly input into the RTC_I pin to replace the crystal. When the external digital clock signal is used to input RTC_I, please note that its signal amplitude should be within 0.9V~1.05V, otherwise it may cause damage to the components of the chip.

3.5.4. Clock Source Combination

Table 3-2 clock source combination

Main clock input	RTC clock input	Description
26MHz TCXO provides clock connection to XTAL_I	32.768kHz crystal provides clock connection to RTC_I and RTC_O	Normal use V_BCKP must be provided by battery to keep RTC running
26MHz TCXO provides clock connection to XTAL_I	32.768kHz external digital signal to RTC_I	Normal use V_BCKP must be provided by battery to keep RTC running
26MHz TCXO provides clock connection to XTAL_I	No clock input	If you do not use the RTC, then connect RTC_O to ground and leave RTC_I floating. Under this

Main clock input	RTC clock input	Description
		condition, GNSS hot-start function is disabled.

For the application of the above clock source combination, the following should be noted in the design:

- When using 26MHz TCXO, the TCXO can be powered by LDO_X, while it is highly recommended to use an external low-noise LDO.
- When 32.768kHz external digital signal is used as the RTC clock, its waveform amplitude must be attenuated to $0.9V_{p-p}$~$1.05V_{p-p}$, with its maximum not higher than 1.05V and the minimum not lower than -0.2V. The clock drift should between ±0.6Hz, 20ppm.

3.6. Power Management Unit (PMU)

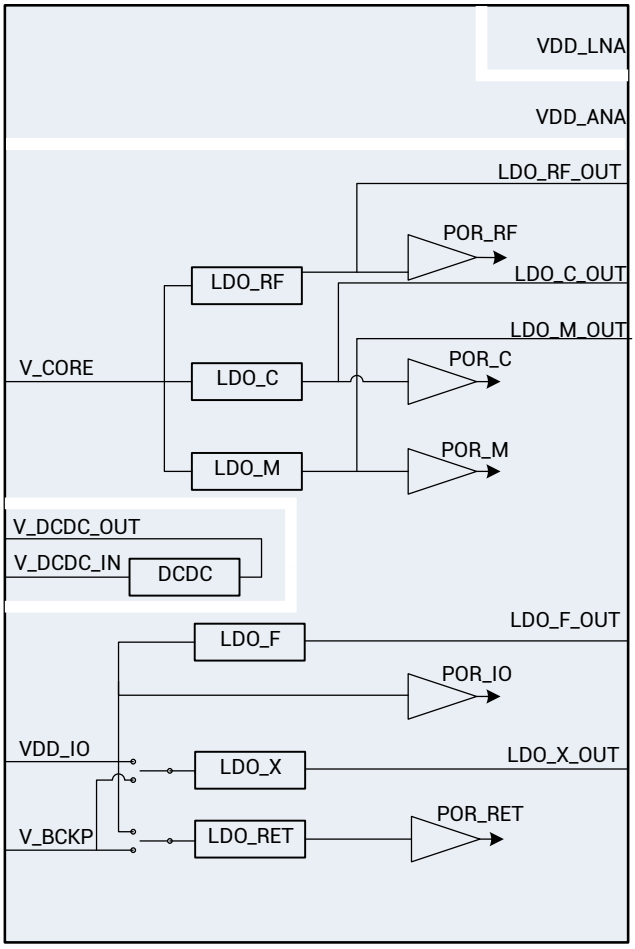


Figure 3-1 Power Management Unit (PMU)

The PMU provides four power domains that are internally generated by LDOs and supervised by several voltage monitors:

- Core

The core domain is the main power domain for the RF and logic inside the chip. Two subsequent LDOs (LDO_C and LDO_RF) convert V_CORE source to respective voltages, which must be decoupled through LDO_C_OUT and LDO_RF_OUT pins respectively. The LDO_C drives the digital logic parts, and the LDO_RF drives the RF and analog circuits.

LDO_RF_OUT does not directly connect or drive RF circuits on-chip. Instead, users should connect it to the VDD_LNA and VDD_ANA on PCB to feed the supply into the on-chip RF circuits. It is recommended to use noise-resistant connections to improve RF performance, such as using magnetic beads.

The power supply of UC6226NIS-E2 adopts DC/DC bypass mode, and the allowable input voltage range of V_CORE is from 1.2V to 1.98V.

- IO

The IO power domain is powered by VDD_IO, including chip IO devices, on-chip Flash, ADC converters and eFuse. The supply voltage of VDD_IO is 1.8V centered (1.77V-1.88V). Except IO pads, the other devices are powered by a dedicated LDO_F to ensure 1.8V supply voltage for on-chip flash, ADC and eFuse. The LDO_F must be connected with a decoupling capacitor through LDO_F_OUT pin.

- Backup

The backup domain runs the RTC section and the Retention RAM. This domain uses the voltage sources of VDD_IO and V_BCKP. In case VDD_IO voltage is inside the normal range, it uses VDD_IO, otherwise use V_BCKP. The allowed voltage range of V_BCKP is 1.65V~3.6V.

- TCXO

If using 26MHz TCXO and TCXO is powered by LDO_X, LDO_X_OUT should be connected to the power pin of TCXO and decoupling capacitance. And user can also choose an external power source other than LDO_X to make TCXO work. Note that if TCXO used as the main clock source, and the clock source is used to drive RTC, do not design the hardware backup function, V_BCKP can't provide the working current required by TCXO.

3.6.1. DC/DC Bypass Mode

The power supply of UC6226NIS-E2 adopts DC/DC bypass mode to ensure high performance. In this mode, both of V_DCDC_IN and V_DCDC_OUT should be connected to V_CORE. The allowable input voltage range for V_DCDC_IN/V_CORE is from 1.2V to 1.98V. The UC6226 chip will be damaged if power supply exceeds the maximum allowable voltage range.

For all power supply, the voltage ripple should not exceed 50mV.

Chapter 4

4. Operating Modes

4.1. Continuous Tracking Mode

Under the full-speed operation mode, the chip's hardware tracking channel will uninterruptedly process satellite signals, to ensure the accuracy of positioning, velocity, and TTFF through high-quality signal acquisition and tracking.

4.2. Sleep Mode

The chip is powered off except for the RTC time keeping unit and Backup RAM. Users can easily wake up according to actual needs. Under the sleep mode, the chip operates at very low power levels and can realize hot start quickly after waking up.

Chapter 5

5. System Configuration

5.1. Configure the Communication Interface

The standard communication interface of UC6226NIS-E2 includes two UART serial ports.

5.2. Configuration Pins

There are two configuration pins: BOOT_MODE (PIO12) and D_SEL (PIO10). When the chip is powered on, the two pins should be pulled up.

5.3. System Reset

According to the power structure of the chip, there are two reset domains: the Core domain and the Backup domain. The Core domain contains all circuits clocked by 26MHz clock, and Backup domain contains RTC circuits and Retention RAM.

The main RESET controls the reset of the Core domain, and the main RESET domain has the following reset sources:

- POR_IO is used to detect the IO voltage. When the IO voltage is lower than 1.7V (1.8V IO supply), the reset signal will be sent to the Core domain.
- POR_DCDC is used to detect the DC/DC input voltage. In the DC/DC bypass mode, when the voltage is less than 1.2V, the reset signal will be sent to the Core domain;
- POR_C is used to detect the core voltage. When the core voltage is less than 90% of the firmware preset voltage, the reset signal will be sent to the Core domain;
- POR_RET is used to detect the voltage of the backup power domain. When the voltage of backup power domain is less than 0.6V, the reset signal will be sent to the Core domain;
- RESET_N is the reset pin of the chip, when its level is low, the reset signal will be sent to the Core domain;
- The reset signal of the software system is controlled by the firmware;
- Watchdog RESET.

If any of the above reset sources issues a Core domain reset signal, the Core domain will be reset.

The Backup RESET domain has the following reset sources:

- POR_RET is used to detect the supply voltage of backup power domain;
- The RTC RESET signal is a soft reset which is controlled by the firmware.

If any of the above reset sources issues a backup domain reset signal, the backup domain will be reset.

5.4. Power on Sequence

The power supply of the chip bypasses the internal DC/DC converter. The RTC region and VDD_IO region are independent of the main power supply, and the power-on sequences do not affect or depend on each other.

It should be noted that after the chip is powered on, a start-up time of more than 230ms must be guaranteed. If the power is cut off in less than 230ms, the chip may work abnormally and V_BCKP may consume more power.

5.4.1. Power-on and Sequence of DC/DC Bypass Mode

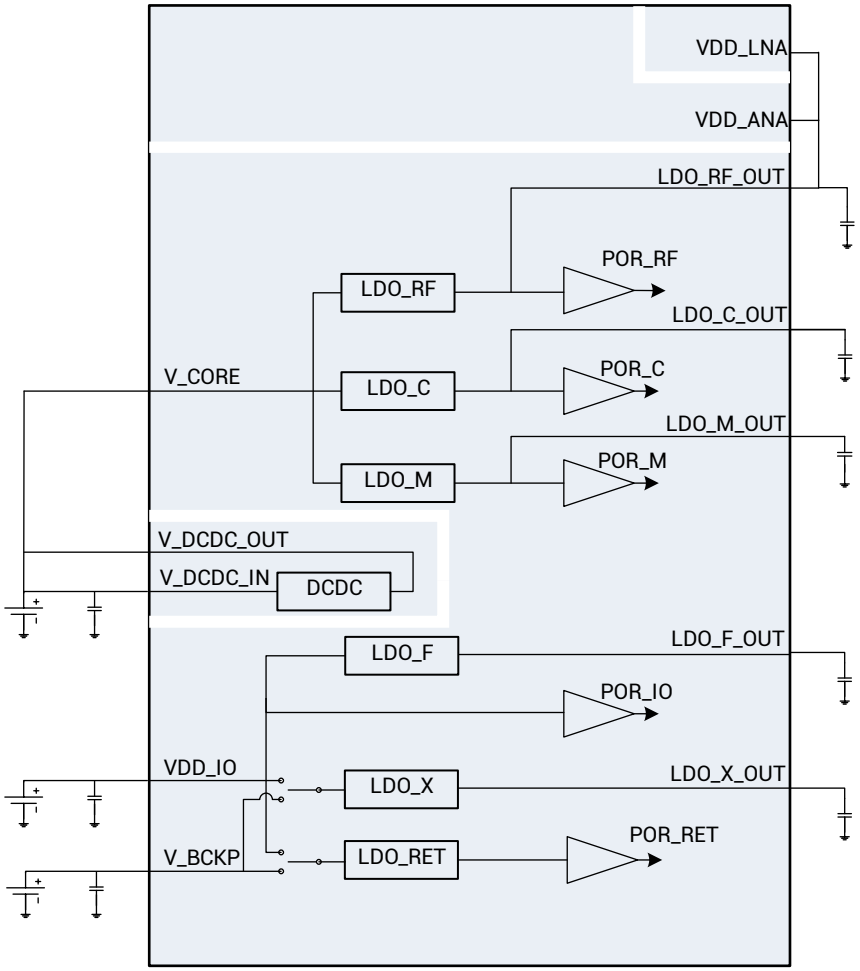


Figure 5-1 Power-on and sequence of DC/DC bypass (Main Supply is 1.2V ~ 1.98V)

In the DC/DC bypass mode, connect the main supply to V_DCDC_IN, V_DCDC_OUT and V_CORE pins, which is independent of VDD_IO.

☞ *Please pay attention that the allowed input voltage of main supply in this mode is limited to 1.2V –1.98V. The supply voltage higher than 1.98V will cause permanent damage of UC6226NIS-E2 chip.*

The power on time for main supply and the VDD_IO should be shorter than 10ms and the power supply ramp should be monotonic. There is no sequence requirement for the main supply and the VDD_IO. However, the missing of any of these two supplies will keep the chip in reset state.

When V_BCKP continues to power, the status of the main supply or VDD_IO does not affect the status of RTC region.

5.4.2. Power on Sequence for Backup Region

The Backup region is powered by the output of an internal power switch, which switches between the IO supply from VDD_IO pin and the backup supply from V_BCKP pin. In order to minimize the backup battery consumption, only when the VDD_IO is powered off does the switch change to V_BCKP supply.

If neither VDD_IO nor V_BCKP is powered, the backup region does not work. If any one of pins is supplied, the backup region will be reset and soon start to be functional.

Chapter 6

6. Pin Definitions

6.1. Pin Distribution

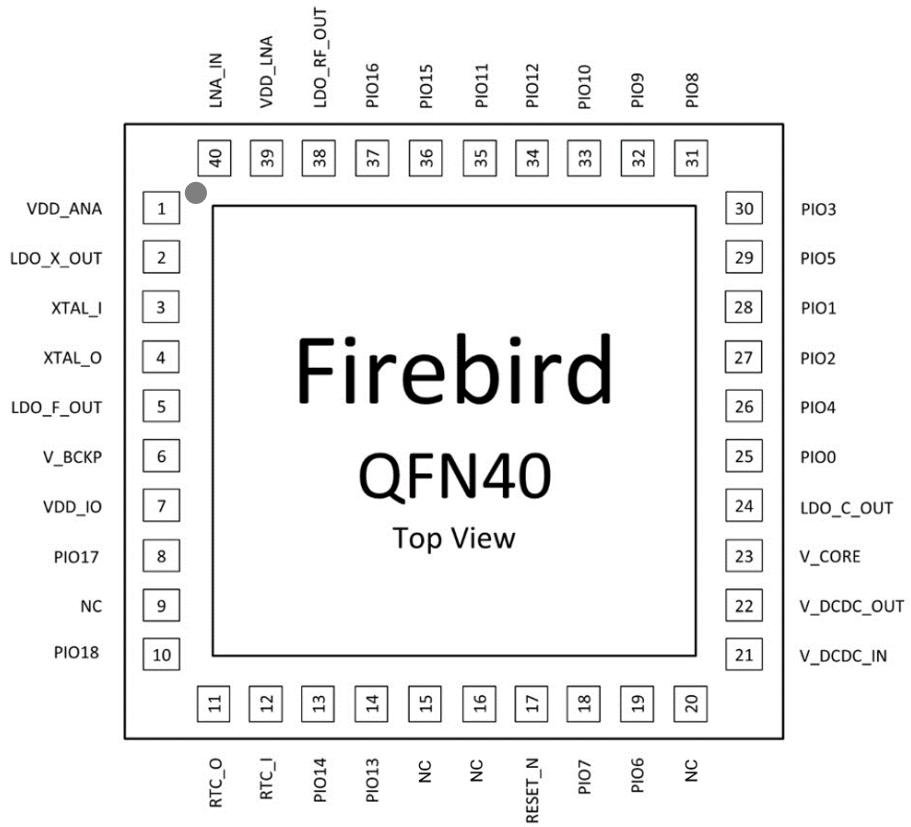


Figure 6-1 QFN40 pin diagram

6.2. Pin Description

Table 6-1 Description of QFN40 Power Supply Pin

Name	Pin	Power Domain	Description
V_DCDC_IN	21	DC/DC	DC/DC input
V_DCDC_OUT	22	DC/DC	DC/DC output
V_CORE	23	Core	Core supply
V_BCKP	6	Backup	Backup cell supply
VDD_IO	7	IO	I/O, TCXO and Flash power supply
VDD_ANA	1	Core/RF	Power supply of analog section
VDD_LNA	39	Core/RF	LNA power supply
LDO_RF_OUT	38	Core/RF	RF power output
LDO_C_OUT	24	Core/Logic	Core power output
LDO_X_OUT	2	Clock	TCXO/crystal power output
LDO_F_OUT	5	Flash	Flash power output
PADDLE	paddle		Ground

Table 6-2 Description of QFN40 Analog Pin

Name	Pin	Power Domain	Description
LNA_IN	40	RF	LNA input (LNA requires an external input matching)
XTAL_I	3	Clock	26MHz TCXO clock input
RTC_I	12	Backup	32.768kHz crystal or digital clock signal input
RTC_O	11	Backup	32.768kHz clock output
RESET_N	17	IO	System reset
NC	/	N/A	NC, please keep float

Table 6-3 Description of QFN40 PIO Pin

Name	Pin	Power Domain	I/O Reset	I/O Core off	Description
PIO0	25	IO	I/pull-up	I/pull-up	IO PIO0
PIO1	28	IO	I/pull-up	I/pull-up	IO PIO1
PIO2	27	IO	I/pull-up	I/pull-up	IO PIO2
PIO3	30	IO	I/pull-up	I/pull-up	IO PIO3
PIO4	26	IO	I/pull-up	I/pull-up	IO PIO4
PIO5	29	IO	I/pull-up	I/pull-up	IO PIO5
PIO6	19	IO	O/pull-up	I/pull-up	IO PIO6
PIO7	18	IO	I/pull-up	I/pull-up	IO PIO7
PIO8	31	IO	I/pull-up	I/pull-up	IO PIO8
PIO9	32	IO	I/pull-up	I/pull-up	IO PIO9
PIO10	33	IO	I/pull-up	I/pull-up	IO PIO10 or D_SEL
PIO11	35	IO	I/pull-up	I/pull-up	IO PIO11
PIO12	34	IO	I/pull-up	I/pull-up	IO PIO12 or BOOT_MODE
PIO13	14	IO	I/pull-down	I/pull-down	IO PIO13
PIO14	13	IO	I/pull-down	I/pull-down	IO PIO14
PIO15	36	IO	I/pull-up	I/pull-up	IO PIO15
PIO16	37	IO	I/pull-up	I/pull-up	IO PIO16
PIO17	8	IO	I/pull-up	I/pull-up	IO PIO17
PIO18	10	IO	I/pull-up	I/pull-up	IO PIO18

Chapter 7

7. Electrical Specifications

7.1. Maximum Absolute Rating

Table 7-1 Maximum absolute rating

Symbol	Parameter		Min.	Max.	unit
V_DCDC_IN	Input voltage of the internal DC/DC converter Connect it to V_CORE to bypass the internal DC/DC		-0.2	1.98	V
V_CORE, V_DCDC_OUT	Supply voltage of baseband main core and RF LDO input Output voltage of the internal DC/DC converter, connect it to V_CORE to bypass the internal DC/DC		-0.2	1.98	V
VDD_IO	VDD_IO_1.8V	VIL	-0.2	0.6	V
		VIH	1.2	1.88	
V_BCKP	Supply voltage of backup domain and LDO_X inputs		-0.2	3.6	V
VDD_ANA, VDD_LNA	Supply voltage RF domain		-0.2	0.99	V
Vi	Input voltage on XTAL_I		-0.2	1.05	V
Vi_{ana}	Input voltage on RTC_I		-0.2	1.05	V
Vi_{dig}	Input voltage on PIO0-18 and RESET_N		-0.2	3.6	V
P_{rfin}	RF input power on LNA_IN			+15	dBm
P_{tot}	Total power			100	mW
T_{jun}	Junction temperature		-40	+125	°C

Symbol	Parameter	Min.	Max.	unit
T_s	Storage temperature	-50	+150	°C
ESD	HBM	-2000	2000	V

7.2. Working Conditions

Table 7-2 QNF40 working conditions

Symbol	Parameter	Min.	Typical	Max.	unit
T_{amb}	Ambient temperature	-30	+25	+85	°C
V_DCDC_IN[7]	Connect to V_CORE under DC/DC bypass mode	1.2	1.8	1.98	V
V_CORE[8]	Supply voltage of baseband main core and RF LDO inputs	1.2	1.8	1.98	V
VDD_IO[9]	Supply voltage of I/O, LDO_X and flash	1.77	1.8	1.88	V
V_BCKP	Supply voltage of backup domain and LDO_X inputs	1.65	3.3	3.6	V
VDD_ANA[10], VDD_LNA	Supply voltage of RF domain	0.65	0.7	0.75	V
F_{ref}	Reference clock		26		MHz

[7] In order to make sure the chip starts normally, V_DCDC_IN and VDD_IO should be lower than 0.4V before starting up.

[8] Connect V_DCDC_IN and V_DCDC_OUT to V_CORE

[9] The voltage ripple should be within 50 mV, and the VDD_IO in the table above does not include the ripple voltage.

[10] In general, VDD_ANA and VDD_LNA should be powered by LDO_RF_OUT. If other design is required, please contact Unicore to obtain technical support.

7.2.1. DC Electrical Characteristics

Table 7-3 DC electrical characteristics

Symbol	Parameter	Min.	Typical	Max.	unit	Condition
VDD_IO[11]	Supply voltage for PIOs and input voltage for LDO_F and LDO_X	1.77	1.8	1.88	V	-30°C ~ +85°C
V_DCDC_IN	Input voltage for DC/DC converter	1.2	1.8	1.98	V	
V_CORE (Internal DC/DC is not used)	Input voltage for LDO_C and LDO_RF	1.2	1.8	1.98	V	
V_BCKP	Input voltage for LDO_B and LDO_X (backup mode)	1.65	3.3	3.6	V	
$I_{LDO\_X\_OUT}$	LDO_X output current			5	mA	
LDO_X_OUT	LDO_X output voltage (With 26MHz TCXO)		-	VDD_IO-0.1	V	
LDO_RF_OUT[12]	LDO_RF output voltage	0.65	0.7	0.75	V	
LDO_F_OUT[13]	LDO_F output voltage = VDD_IO input voltage – 100 mV				V	
LDO_C_OUT[14]	LDO_C output voltage	0.80		0.95	V	
VDD_ANA	Power supply pin	0.65	0.7	0.75	V	
VDD_LNA	Power supply pin	0.65	0.7	0.75	V	
I_{PPS}	PPS Output Current[15]			4	mA	

[11] The voltage ripple should be within 50 mV, and the VDD_IO in the table above does not include the ripple voltage.

[12] [13] [14] If external voltage supply is needed, please contact Unicore Communications, Inc.

[15] Without external resistor

7.2.2. Analog Parameters

Table 7-4 Analog parameters

Symbol	Parameter	Condition	Min.	Typical	Max.	unit
RTC_Fxtal	RTC crystal oscillator resonant frequency			32768		Hz
RTC_T_start	RTC startup time		0.2	1	2	s
RTC_Iosc	32.768 kHz OSC current source			3		μA
RTC_Amp	32.768 kHz OSC amplitude	ESR = 80 kΩ	50		350	mVpp
RTC_ESR	32.768 kHz Xtal equivalent series resistance				90	kΩ
RTC_CL	RTC integrated load capacitance	ESR = 80 kΩ	7	12.5	12.5	pF
RTC_Vil	RTC low level input voltage	Shared RTC oscillator input	0.0		0.2	V
RTC_Vih	RTC high level input voltage	Shared RTC oscillator input	0.7		0.9	V

7.2.3. RF Parameters

Table 7-5 RF parameters

Symbol	Parameter	Condition	Min.	Typical	Max.	unit
Fin	Receiver input frequency		1550	1575.42	1620	MHz
LNA_IN	LNA input impedance	Require matching devices and DC blocking capacitors. Matching device typical value: series inductance L = 7.5nH, ground capacitance C = 3pF.		50		Ω

Symbol	Parameter	Condition	Min.	Typical	Max.	unit
		The typical value of DC blocking capacitor is 47pF.				
LNA_S11	LNA input return loss	50Ω environment		-10		dB
NFtot	Receiver chain noise figure	50Ω environment		2.5		dB
Ext_Gain	External gain before matching	50Ω environment			45	dB
TCXO_Freq	TCXO frequency			26		MHz
TCXO_IN_Vpp	TCXO input peak-to-peak voltage		0.3	0.6	1	V_{pp}

7.2.4. Current Consumption

Table 7-6 Current consumption

Symbol	Parameter	Condition	Typical	unit
I_{BCKP}	V_BCKP backup current using the RTC crystal	Retention RAM powered (V_BCKP = 3.6V, VDD_IO = V_CORE = 0V)	70	μA

7.3. Reference Power Requirements

The table below lists examples of the total system supply current including RF and baseband section for a possible application.

Values listed below are provided for customer information only as an example of typical current requirements (the basic frequency of system is 66MHz). Values are characterized on samples – actual power requirements can vary depending on Firmware version used, external circuitry, number of SVs tracked, signal strength, type and time of start, duration, and conditions of test.

Table 7-7 Reference power requirements

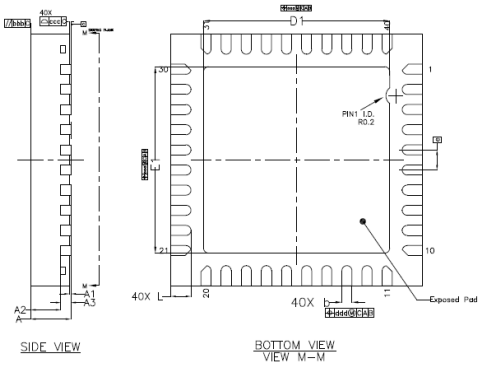
Symbol	Parameter	Condition	Typical	unit
I_{vdd_io}	IO current	V_CORE=0V No external peripherals	100@1.8V	uA
I_{V_CORE}	V_CORE = 1.8 V (the core domain is powered by the internal LDOs)	Acquisition (GNSS dual mode)	48	mA
		Tracking (GNSS dual mode, continuous tracking)	26	
		Tracking (GNSS single mode, continuous tracking)	24	

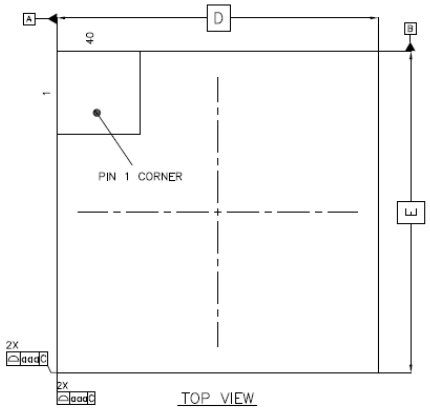
☞ *GNSS dual mode, supports GPS+BDS or GPS+GLONASS dual-system joint positioning; GNSS single mode, supports GPS, BDS or GLONASS standalone positioning.*

☞ *UC6226NIS-E2 operating current is related to firmware characteristics, including operating frequency, voltage, GNSS software strategy, etc. The above parameters are measured at 66MHZ system frequency. For further details, please refer to relevant test report.*

Chapter 8

8. Mechanical Specifications





DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0.00	---	0.05
MOLD THICKNESS		A2	0.50	0.55	0.60
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D	4.90	5.00	5.10
	Y	E	4.90	5.00	5.10
LEAD PITCH		e	0.40 BSC		
EP SIZE	X	D1	3.65	3.70	3.75
	Y	E1	3.65	3.70	3.75
LEAD LENGTH		L	0.35	0.40	0.45
Tolerance of form and position					
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

Figure 8-1 QFN40 Mechanical Parameters

Chapter 9

9. Reliability Test and Certificate

9.1. Reliability Test

UC6226NIS-E2 chips are qualified with appropriate JEDEC standards, e.g. JESD47 Stress-Test-Driven Qualification of Integrated Circuits.

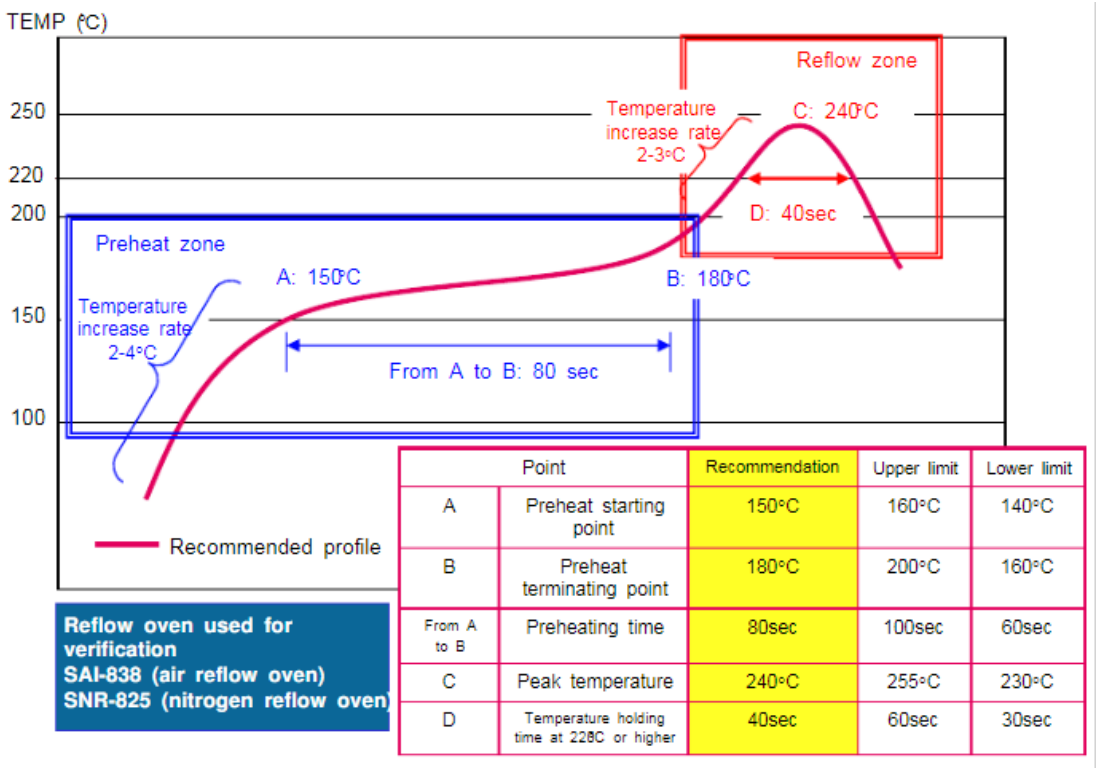
9.2. Certificate

Products marked with lead-free symbol on the product label comply with the “Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment". UC6226NIS-E2 chips are RoHS and REACH compliant.

Chapter 10

10. Reflow Soldering

The reflow soldering temperature curve is recommended as shown in Figure 10-1 below (M705-GRN360 is recommended for solder paste).



Point		Recommendation	Upper limit	Lower limit
A	Preheat starting point	150°C	160°C	140°C
B	Preheat terminating point	180°C	200°C	160°C
From A to B	Preheating time	80sec	100sec	60sec
C	Peak temperature	240°C	255°C	230°C
D	Temperature holding time at 228C or higher	40sec	60sec	30sec

Figure 10-1 Reflow Soldering Temperature Curve

Chapter 11

11. Product Appearance and Packaging

11.1. Appearance

Figure 11-1 Product appearance

The appearance of UC6226NIS-E2 is shown in the above picture, the marking information may vary from customer order code, please follow the actual order.

11.2. Label

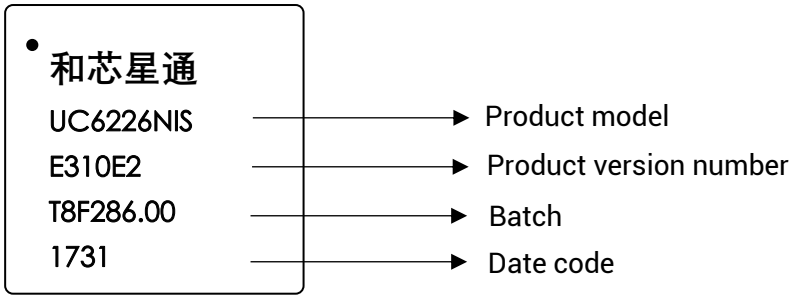


Figure 11-2 Product label description

Table 11-1 Specific description of product label

Code	Description
UC6226	Main model of product
N	Package type code: N - QFN Package
I	Level: I - Industrial grade*
S	Whether containing built-in Flash: S-Flash built-in

Code	Description
E	Internal code
310	Internal code
E2	Efuse configuration number
1731	Production date

11.3. Packaging

UC6226NIS-E2 adopts tape packaging, QFN40 contains 3000 pieces in each package. The packaging is as follows:

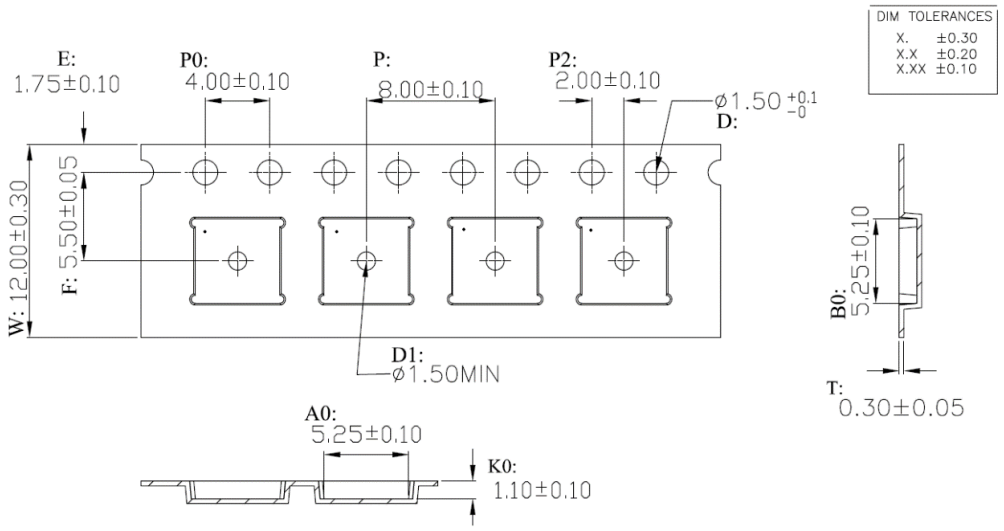


Figure 11-3 UC6226NIS-E2 Tape packaging

Tape specifications are as follows:

1. 10-hole spacing cumulative tolerance is ± 0.20mm;
2. All dimension sizes meet EIA-481-C requirements;
3. Thickness: 0.3 ± 0.05mm

Chapter 12

12. Ordering Codes

Table 12-1 Ordering Codes

Order Number	Description
UC6226NIS	QFN40 package, industrial grade*, built-in Flash, supports firmware update.
-E310E2	VDD_IO input voltage: 1.77V~1.88V[16], and the ambient temperature should be within -30°C to +85°C.

[16] The voltage ripple should be within 50 mV; this range of VDD_IO does not include the ripple voltage.

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